SEMICONDUCTOR DEVICE AND OPERATING METHOD THEREOF

BACKGROUND

[0001] 1. Technical Field

[0002] The disclosure relates in general to a semiconductor device and an operating method thereof, and more particularly to a semiconductor device capable of performing a positive voltage operation and a negative voltage operation and an operating method thereof.

[0003] 2. Description of the Related Art

[0004] Recently, along with the research and developments of semiconductor devices, the demands of high voltage semiconductor devices have rapidly increased. For example, metal oxide semiconductors, such as a lateral diffused MOSFET transistor (LDMOS), capable of withstanding a high voltage have drawn a lot of attention.

[0005] However, the manufacturing process as well as the structure of a LDMOS is critical to its operations and functions. Therefore, there is always a continuing need to provide an improved high voltage semiconductor device as well as the manufacturing process thereof.

SUMMARY OF THE INVENTION

[0006] The disclosure is directed to a semiconductor device and an operating method thereof. According to some embodiments of the present disclosure, the first lightly-doped region is formed below the source region, such that it can stop the lightly-doped region having a different polarity from that of the first lightly-doped region from expanding too much causing punch through between the lightly-doped region and the source region.

[0007] According to an embodiment of the present disclosure, a semiconductor device is disclosed. The semiconductor device includes a substrate, a source region, a drain region, a gate structure, a first lightly-doped region, and a first isolation region. The source region and the drain region are formed in the substrate. The gate structure is formed on the substrate and between the source region and the drain region. The first lightly-doped region is formed below the source region. The first isolation region is formed in the substrate and surrounding the source region, the drain region, and the first lightly-doped region. The source region and the drain region have a first-polarity, and the first lightly-doped region and the first isolation region have a second-polarity.

[0008] According to another embodiment of the present disclosure, an operating method of a semiconductor device is disclosed. The operating method includes the following steps: providing the semiconductor device, which comprises a substrate, a source region, a drain region having a first voltage, a gate structure, a first lightly-doped region, an isolation doped region having a second voltage, and a doped region; applying a positive voltage to the gate structure when the first voltage is equal to the second voltage, and the source region and the doped region are grounded; and applying a negative voltage to the gate structure when the first voltage is different from the second voltage, the source region has a negative voltage, and the doped region is grounded. The source region and the drain region are formed in the substrate, and the gate structure is formed on the substrate and between the source region and the drain region. The first lightly-doped region is formed below the source region, and the isolation doped region is formed in the substrate and surrounding the source region, the drain region, and the first lightly-doped region. The doped region is formed in the substrate and located outside the isolation doped region. The source region and the drain region have a first-polarity, and the first lightly-doped region the isolation doped region, and the doped region have a second-polarity

[0009] The disclosure will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. **1**A shows a top view of a semiconductor device according to an embodiment of the present disclosure;

[0011] FIG. **1**B shows a cross-sectional view along the section line **1**B-**1**B' in FIG. **1**A;

[0012] FIG. **2**A shows a top view of a semiconductor device according to another embodiment of the present disclosure;

[0013] FIG. **2**B shows a cross-sectional view along the section line **2**B-**2**B' in FIG. **2**A; and

[0014] FIGS. **3**A-**3**B show I-V curves of a semiconductor device according to the embodiments of the present disclosure under positive voltage operation and negative voltage operation, respectively.

DETAILED DESCRIPTION OF THE INVENTION

[0015] In some embodiments of the present disclosure, in the semiconductor device, the first lightly-doped region is formed below the source region, such that it can stop the lightly-doped region having a different polarity from that of the first lightly-doped region from expanding too much causing punch through between the lightly-doped region and the source region. The embodiments are described in details with reference to the accompanying drawings. The procedures and details of the method of the embodiments are for exemplification only, not for limiting the scope of protection of the disclosure. Moreover, the identical elements of the embodiments are designated with the same reference numerals. Also, it is also important to point out that the illustrations may not be necessarily be drawn to scale, and that there may be other embodiments of the present disclosure which are not specifically illustrated. Thus, the specification and the drawings are to be regard as an illustrative sense rather than a restrictive sense.

[0016] FIG. **1**A shows a top view of a semiconductor device **100** according to an embodiment of the present disclosure, and FIG. **1**B shows a cross-sectional view along the section line **1**B-**1**B' in FIG. **1**A. Referring to FIGS. **1**A-**1**B, the semiconductor device **100** includes a substrate **110**, a source region **120**, a drain region **130**, a gate structure **140**, a first lightly-doped region **150**, and a first isolation region **160**. The source region **120** and the drain region **130** are formed in the substrate **110**. The gate structure **140** is formed on the substrate **110** and between the source region **120** and the drain region **130**. The first lightly-doped region **150** is formed below the source region **120**. The first isolation region **160** is formed in the substrate **110** and surrounding the source region **120**, the drain region **130**, and the first lightly-doped region **150**. The source region **120** and the drain region **130** have a first-polarity, and the first lightly-doped region **150** and the first isolation region **160** have a second-polarity. In the embodiment, the first lightly-doped region **150** is such as a high voltage P-type lightly-doped region (HV_PLDD),